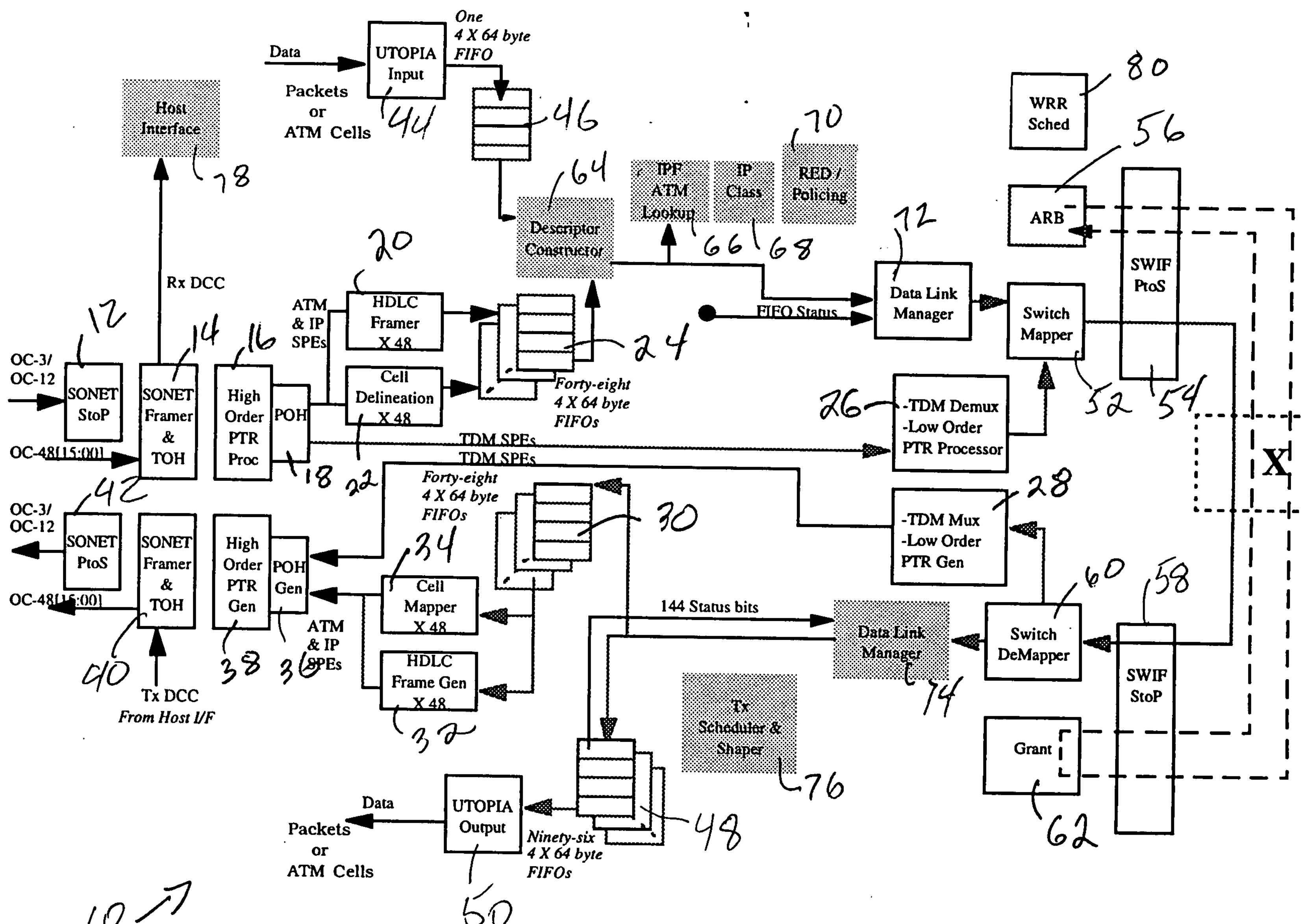


Data
Packets or ATM Cells
UTOPIA Input
44
One 4 X 64 byte FIFO
46
Host Interface
78
Rx DCC
Descriptor Constructor
64
IPF ATM Lookup
IP Class
RED / Policing
66
68
70
WRR Sched
80
ARB
56
SWIF PtoS
54
X
OC-3/ OC-12
SONET StoP
12
OC-48[15:00]
SONET Framer & TOH
14
High Order PTR Proc
16
POH
18
ATM & IP SPEs
HDLC Framer X 48
20
Cell Delineation X 48
22
Forty-eight 4 X 64 byte FIFOs
24
FIFO Status
Data Link Manager
72
Switch Mapper
52
-TDM Demux -Low Order PTR Processor
26
TDM SPEs
TDM SPEs
-TDM Mux -Low Order PTR Gen
28
OC-3/ OC-12
SONET PtoS
42
OC-48[15:00]
SONET Framer & TOH
40
Tx DCC From Host I/F
High Order PTR Gen
38
POH Gen
36
ATM & IP SPEs
Forty-eight 4 X 64 byte FIFOs
30
Cell Mapper X 48
34
HDLC Frame Gen X 48
32
144 Status bits
Data Link Manager
74
Switch DeMapper
60
SWIF StoP
58
Grant
62
Tx Scheduler & Shaper
76
Ninety-six 4 X 64 byte FIFOs
48
UTOPIA Output
50
Data
Packets or ATM Cells
10

Fig-1

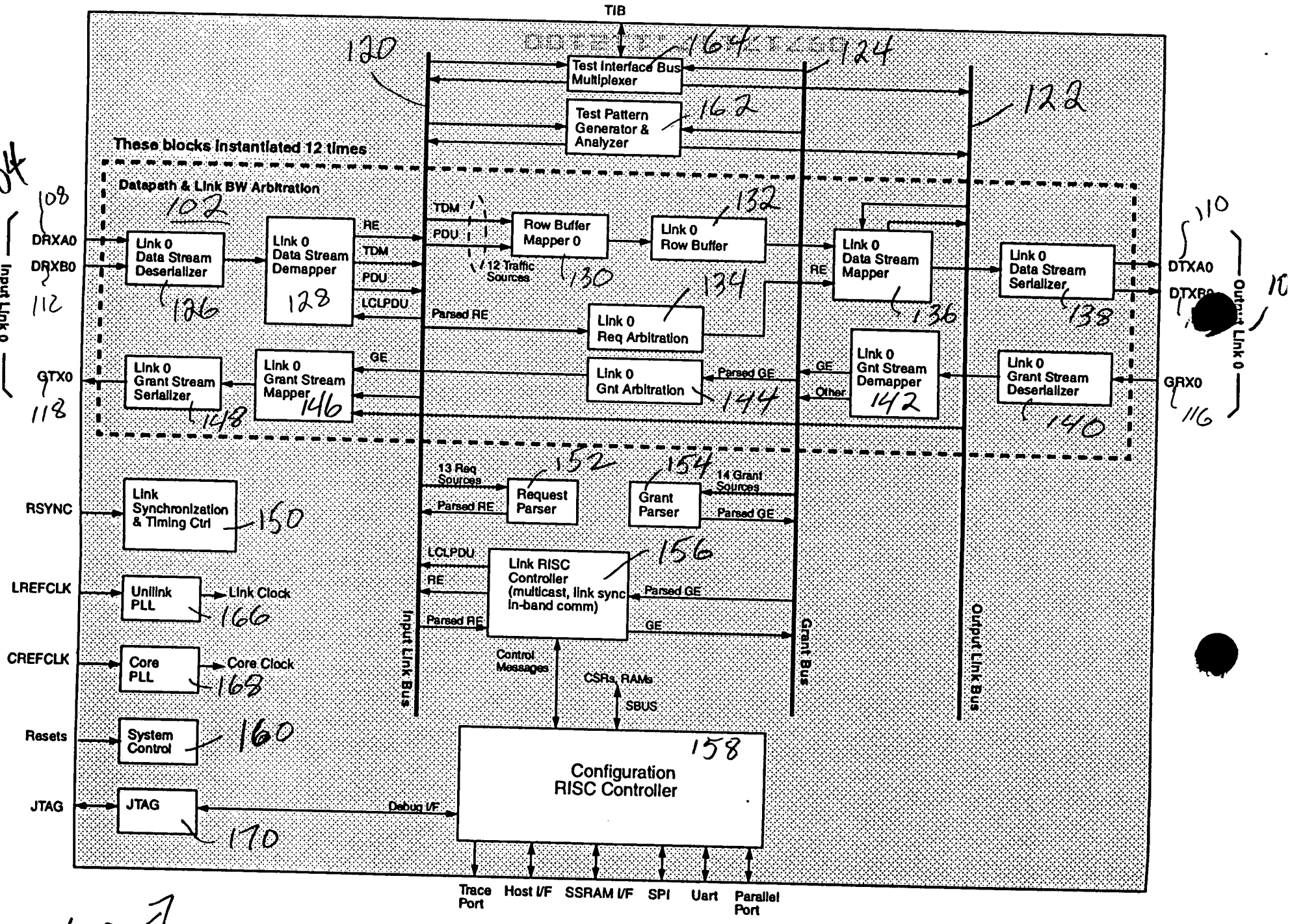
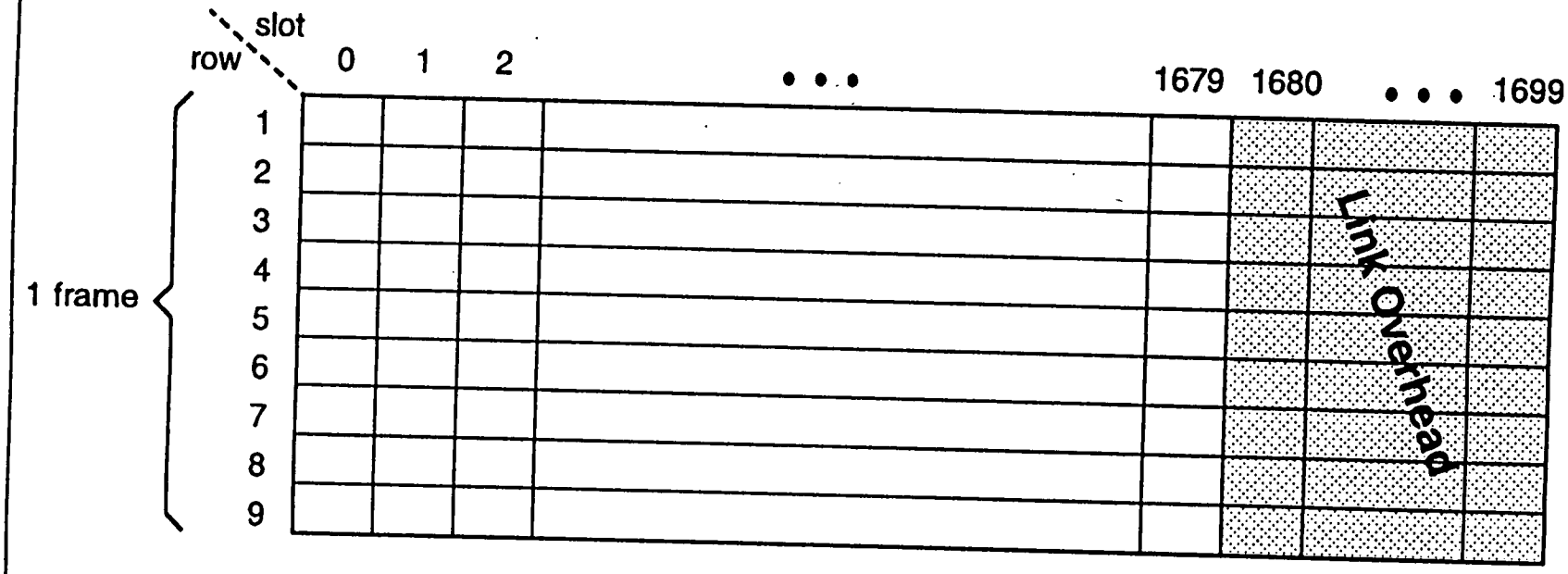

TIB
120
164
124
Test Interface Bus Multiplexer
Test Pattern Generator & Analyzer
162
122
These blocks instantiated 12 times
104
Datapath & Link BW Arbitration
102
108
DRXA0
DRXB0
112
Input Link 0
Link 0 Data Stream Deserializer
126
Link 0 Data Stream Demapper
128
RE
TDM
PDU
LCLPDU
TDM
PDU
12 Traffic Sources
Row Buffer Mapper 0
130
Link 0 Row Buffer
132
Link 0 Data Stream Mapper
136
Link 0 Data Stream Serializer
138
110
DTXA0
DTXB0
Output Link 0
Parsed RE
Link 0 Req Arbitration
134
RE
GTX0
118
Link 0 Grant Stream Serializer
148
Link 0 Grant Stream Mapper
146
GE
Link 0 Gnt Arbitration
Parsed GE
144
GE
Other
Link 0 Gnt Stream Demapper
142
Link 0 Grant Stream Deserializer
140
GRX0
116
13 Req Sources
Parsed RE
Request Parser
152
Grant Parser
154
14 Grant Sources
Parsed GE
RSYNC
Link Synchronization & Timing Ctrl
150
LCLPDU
RE
Parsed RE
Link RISC Controller (multicast, link sync in-band comm)
156
Parsed GE
GE
LREFCLK
Unilink PLL
Link Clock
166
CREFCLK
Core PLL
Core Clock
168
Input Link Bus
Grant Bus
Output Link Bus
Control Messages
CSRs, RAMs
SBUS
Resets
System Control
160
158
Configuration RISC Controller
JTAG
JTAG
170
Debug I/F
Trace Port
Host I/F
SSRAM I/F
SPI
Uart
Parallel Port
100

Fig. 2



1 frame = 125 us

1 row = 125 us / 9 = 13.89 us

1 slot = 4 bit tag + 32 bit payload

serial bit rate = 1700 slots/row * 36 bits/slot * 9 rows/frame * 8 kHz = 550,800 bits/frame = 4.4064 Gbps

row size = 1700 slots/row = 7,560 bytes/row = 61,200 bits/row

1 slot bandwidth = slot rate * 36 bits/slot = 72 kHz * 36 = 2.592 Mbps

Fig. 3

Slot	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Parity				PDU		0	0	Routing Tag																													
1	Parity				Ver		Valid Bytes						VOQ ID						Frag ID		A		FFS												Seq #			
2	Parity				FFS																Dest Flow ID															
3	Parity				payload byte 0								payload byte 1								payload byte 2								payload byte 3							
4 -	Parity				payload byte 4								payload byte 5								payload byte 6								payload byte 7							
15	Parity				payload byte 48								payload byte 49								payload byte 50								payload byte 51							

Fig. 3a

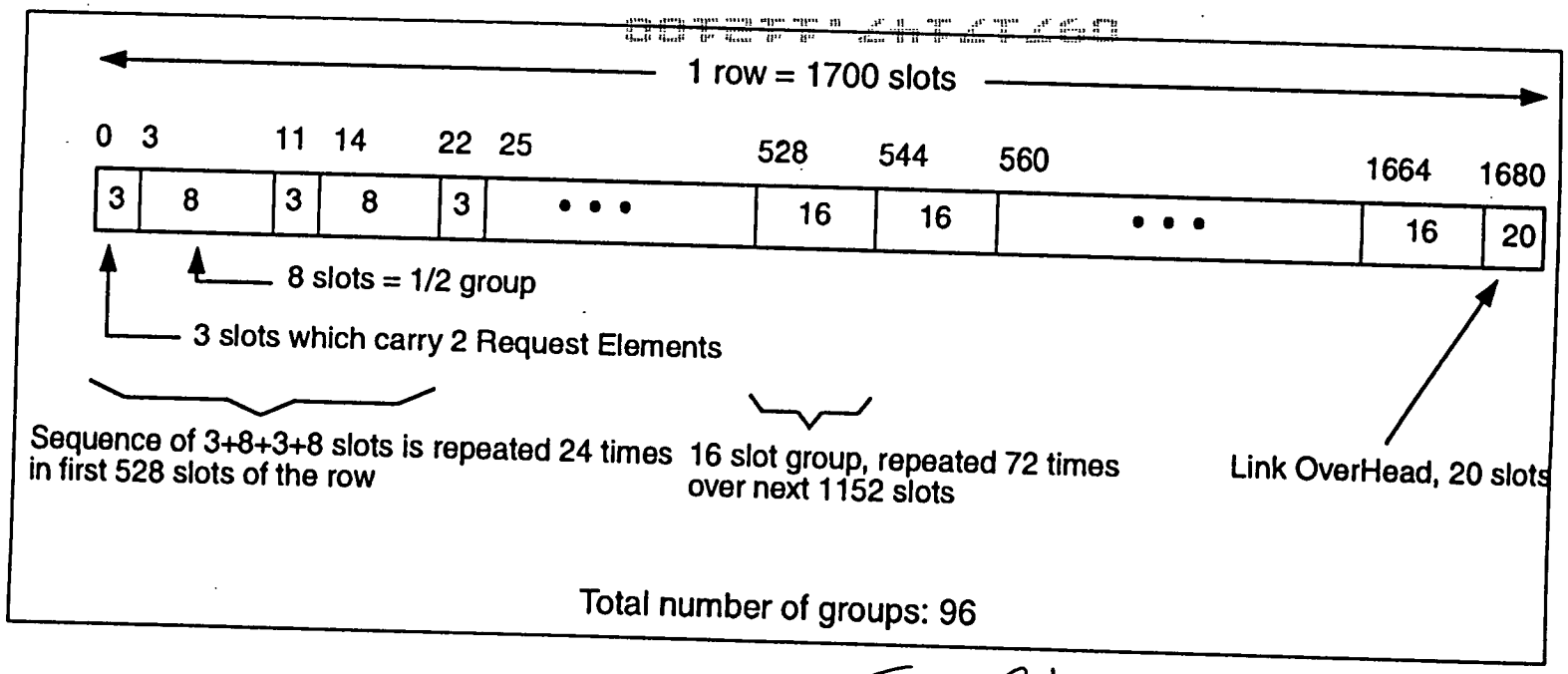

1 row = 1700 slots
0 3 11 14 22 25 528 544 560 1664 1680
3 8 3 8 3 • • • 16 16 • • • 16 20
8 slots = 1/2 group
3 slots which carry 2 Request Elements
Sequence of 3+8+3+8 slots is repeated 24 times in first 528 slots of the row
16 slot group, repeated 72 times over next 1152 slots
Link OverHead, 20 slots
Total number of groups: 96

Fig. 3b

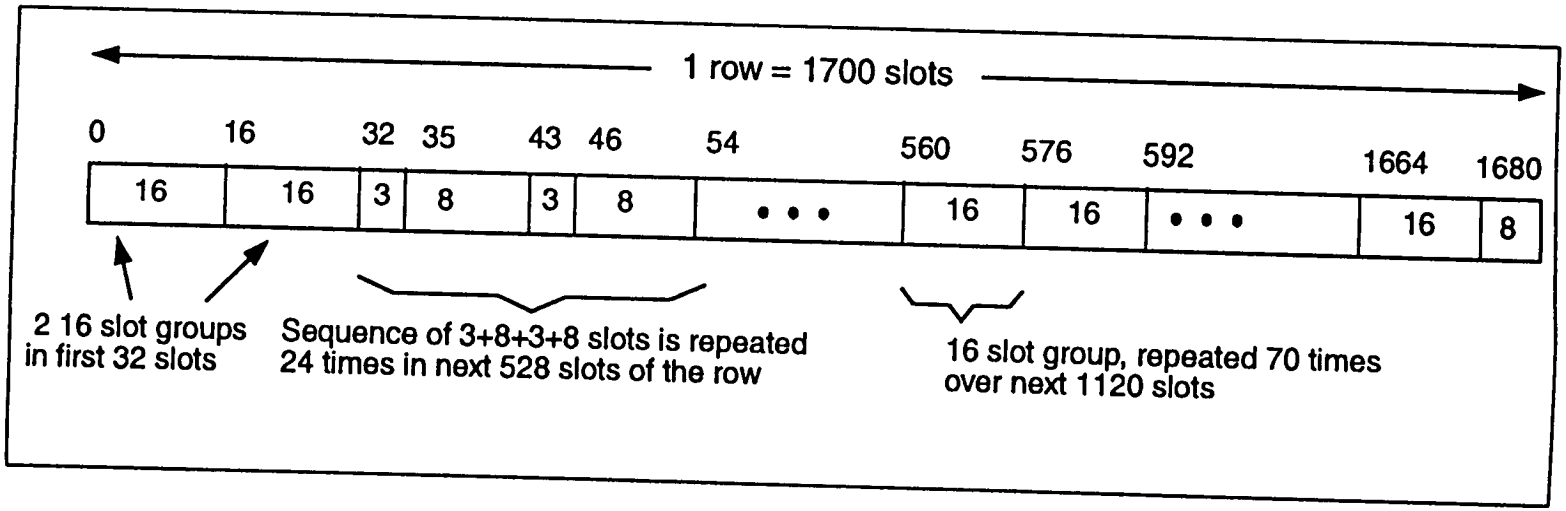

1 row = 1700 slots
0 16 32 35 43 46 54 560 576 592 1664 1680
16 16 3 8 3 8 • • • 16 16 • • • 16 8
2 16 slot groups in first 32 slots
Sequence of 3+8+3+8 slots is repeated 24 times in next 528 slots of the row
16 slot group, repeated 70 times over next 1120 slots

Fig. 3c

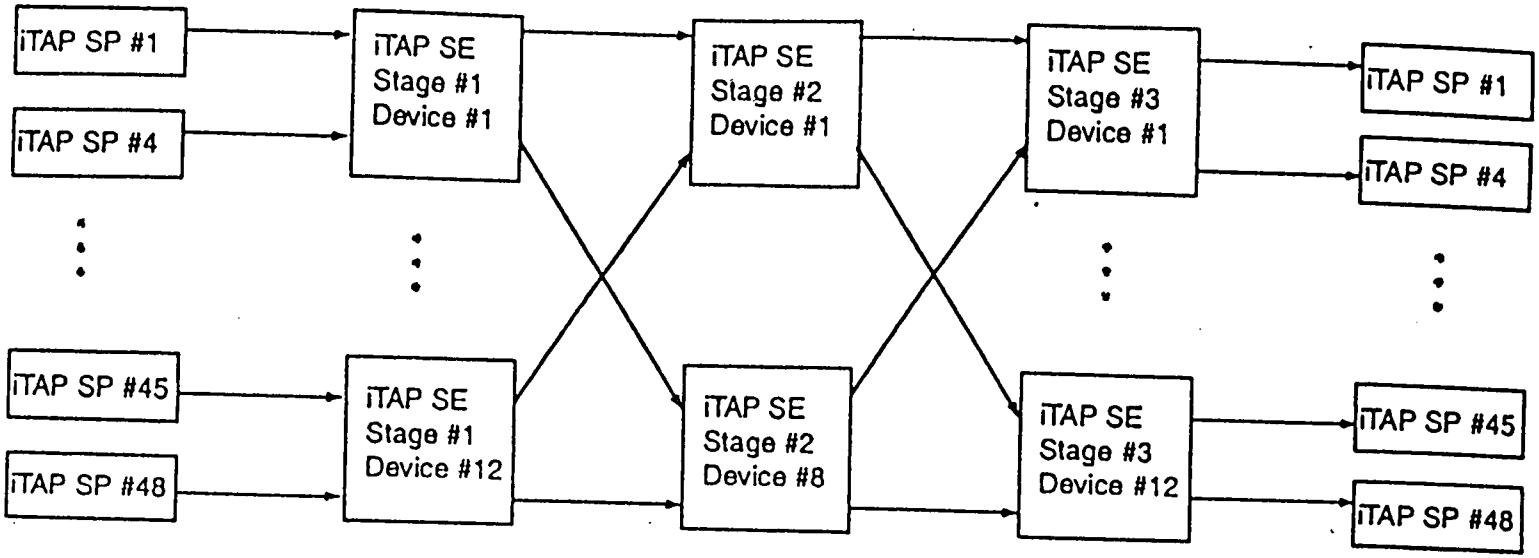


Fig. 4

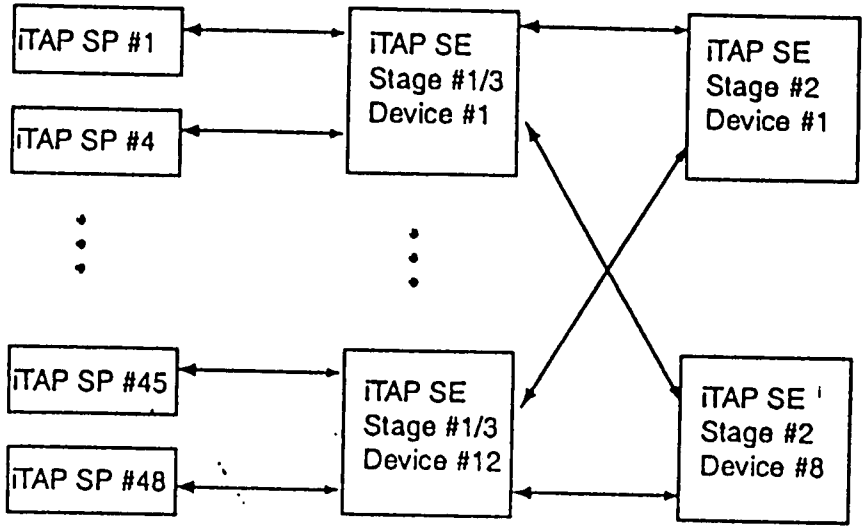


Fig. 5